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Reg. No. : .....

Name : .....

Eighth Semester B.Tech. Degree Examination, May 2013
(2008 Scheme)
08.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

(Answer **all** questions)

1. Distinguish between register-to-register and memory-to-memory architecture for building conventional multivector supercomputers.
2. Describe different types of hazards due to data dependency.
3. Briefly describe differences among UMA, NUMA and COMA model.
4. Explain how instruction set and memory hierarchy affect the CPU performance in terms of clock rate, program length and effective CPI ?
5. What is meant by Hit ratio and page fault ?
6. Describe the cache inconsistencies caused by process migration.
7. Justify the statement : "Multiple functional units as well as Hazard avoidance improve throughput of pipelined processor".
8. Distinguish between static and dynamic interconnection network.
9. Distinguish between multiprocessors and multicomputers.
10. Compare fine-grained and coarse-grained SIMD architecture. **(10×4=40 Marks)**

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PART – B

(**Each** question carries **20** marks)

11. Consider the execution of the following code segment consisting of seven statements. Use Bernstein's conditions to detect the maximum parallelism embedded in this code. Justify the portions that can be executed in parallel and the remaining portions that must be executed sequentially. Rewrite the code using parallel constructs such as Cobegin and Coend. No variable substitution is allowed. All statements can be executed in parallel if they are declared within the same block of a (Cobegin, Coend) pair.

S1 : A = B + C

S2 : C = D + E

S3 : F = G + E

S4 : C = A + F

S5 : M = G + C

S6 : A = L+ C

S7 : A = E + A **20**

OR

12. Analyse the data dependences among the following statements in a given program.

S1 : Load R1, M(100) /R1 ← Memory (100)/

S2 : Move R2, R1 /R2 ←(R1)/

S3 : Inc R1 /R1 ← (R1) + 1/

S4 : Add R2, R1 /R2←(R2) + (R1)/

S5 : Store M(100), R1 /Memory(100) ← (R1)/

Where (Ri) means the content of register Ri.

i) Draw dependence graph to show all the dependences.

ii) Are there any resource dependences if only one copy of each functional unit is available in the CPU ? **20**

13. a) Consider the following reservation table for a four stage pipeline with a clock cycle $\tau = 20$ ns.

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

i) What are the forbidden latencies and the initial collision vector ?

ii) Draw the state transition diagram for scheduling the pipeline.

iii) Determine the MAL associated with the shortest greedy cycle.

iv) Determine the pipeline throughput corresponding to the MAL and given τ.

b) Describe the issues in preserving sequential consistency of instruction execution in superscalar processor. **20**

OR

14. a) What is the use of reorder buffer ?

b) Design a binary integer multiply pipeline with five stages. The first stage is for partial product generation. The last stage is a 36-bit carry-lookahead adder. The middle three stages are made of 16 carry-save adders (CSAs) of appropriate lengths.

i) Prepare a schematic design of the five-stage multiply pipeline. All line widths and interstage connections must be shown.

ii) Determine maximal clock rate of the pipeline if the stage delays are $\tau_1 = \tau_2 = \tau_3 = \tau_4 = 90$ ns, $\tau_5 = 45$ ns, and the latch delay is 20 ns.

iii) What is the maximal throughput of this pipeline in terms of the number of 36-bit results generated per second ? **20**

15. Explain :

a) Full map directory based protocol

b) Snoopy bus protocol. **20**

OR

16. a) Explain blocking and non-blocking network with the help of Omega network.

b) Describe data flow and hybrid architecture. **20**